a comparator for generating a difference signal representative of a difference between the first voltage value and the second voltage value.

14. (once amended) Apparatus in accordance with Claim 12 wherein the freeze threshold value is approximately equal 0.05 Vrms, and wherein the fault threshold value is approximately equal 0.08 Vrms.

Remarks

The Office Action mailed April 25, 2001 has been carefully reviewed and the foregoing amendment has been made in consequence thereof. Submitted herewith is a Submission of Marked Up Paragraphs and Claims

Claims 1-18 are pending in this application. Claims 1-18 stand rejected.

The objection to the drawings is respectfully traversed. The specification has been amended at pages 3 and 4 to recite that a memory is not shown, and at page 4 to recite that a comparator is not shown. Applicants respectfully submit that illustrating a memory and a comparator is not necessary for an artisian of ordinary skill in the art to understand the invention, and as such, is not essential for a proper understanding of the disclosed invention.

Furthermore, Applicants respectfully submit that the one pole lag filter is shown. More specifically, the specification recites at page 3, lines 12-14 that "V1 + V2 is fed to two separate simple one pole lag filters, i.e., a short term filter 52 and a long term filter 54." Filters 52 and 54 are illustrated in Figure 2.

Figure 3 has been amended to label the y-axis as "Confidence Factors", and the x-axis has been amended to include unit values of 0.04 for CFHi Thresh and 0.08 for CFLo Thresh. Submitted herewith is a Request For Approval of Drawing Changes incorporating the amendment to the drawings. Upon approval of the drawing changes, Applicants will submit

substitute drawings incorporating the above-noted change. For the reasons set forth above, Applicants request that the objection to the drawings be withdrawn.

The objection to the specification is respectfully traversed. The title has been changed and is more indicative of the invention to which the claims are directed. The specification has been amended at page 3, line 20 to recite "a previous short term". With respect to page 3, lines 24-25, and page 4 line 11, the specification has been amended to recite "memory (not shown)". Furthermore, the specification has also been amended at page 4 to recite "Ltfreeze Thresh represents a long term filter freeze threshold", and at page 5, to recite "V2FLTThresh represents a fault threshold value." In addition, at page 4, line 12, the specification has been amended to recite "long term sum".

At page 5, lines 1, 7, and 10, the specification has been amended to correctly recite "DLTST" rather than "DLST". Additionally, at page 5, the specification has been amended to recite "[f]or Vrms values of the absolute value of DLTST between CFHiThresh and CFLoThresh, a linear relationship between the Vrms value and the confidence factor is provided."

Applicants respectfully submit that an artisian of ordinary skill in the art reading the disclosure, would not need a more detailed description set forth in the specification to understand the phrase "a previous short term", or to understand how to utilize a memory. In addition, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand the term V2FLTThresh represents a fault threshold value that is used to determine further action to be taken, and in light of the specification and the Figures, would also understand the relationship between CFHiThresh, CFLoThresh, and DLTST.

Furthermore, Applicants respectfully submit that illustrating a control system is not necessary for an understanding of the invention. Rather, as recited in the specification at page 3, lines 5-10, Figure 2 is a schematic illustration of an exemplary logic circuit that may be implemented in an on-board interface board that is electrically connected between a transducer

and a controller, or that the logic circuit could form part of an on-board controller. Furthermore, at page 5, the specification recites that the logic circuit could be utilized in a control system to minimize the effect of an LVDT/RVDT failure.

With respect to how the switch position depends from a control signal, and with respect to the confidence factors, Applicants respectfully submit that an artisian of ordinary skill in the art would understand the relationship between the logic circuit and a separate controller, including the transmission of control signals. Furthermore, Applicants submit that one skilled in the art reading the disclosure, including the Figures, would understand how the confidence factors can be utilized in a control system to minimize the effect of an LVDT/RVDT failure.

Furthermore, Applicants respectfully submit that it is not necessary to disclose a more detailed circuit which compares the absolute value of an element to a reference for an artisian of ordinary skill in the art to understand the invention. Accordingly, Applicants respectfully submit that the specification satisfies the requirements of Section 112, and as such, request that the Section 112 rejection of the specification be withdrawn.

The rejection of Claims 1-18 under 35 U.S.C. § 112 is respectfully traversed.

As explained above, the specification of the present application meets the requirements of Section 112. Particularly, with respect to Claims 1 and 11, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand the phrase "maintaining the reference value constant". Applicants also respectfully submit that one skilled in the art would understand the values of LTfreeze and LtfreezeThresh without illustrating the values in the Figures. More specifically, Applicants respectfully submit that one skilled in the art would understand that such values are utilized in describing the relationship between the absolute value of DLTST, Vrms, and an output of the long term filter. Accordingly, Applicants respectfully submit that Claims 1 and 11 overcome the Section 112 first paragraph rejections.

With respect to Claims 2 and 12, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand the phrase "generating a fault indication signal", and would understand the relationship between DLTST, VDTFLT, V1 + V2FLTThresh, and V2FLTThresh. Applicants also respectfully submit that one skilled in the art would understand the values and the relationship between DLTST, VDTFLT, V1 + V2FLTThresh, and V2FLTThresh without illustrating the values in the Figures. Accordingly, Applicants respectfully submit that Claims 2 and 12 overcome the Section 112 first paragraph rejections.

With respect to Claims 3 and 13, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand the phrase "generating a confidence factor" in light of the exemplary values of CFHiThresh and CFLoThresh illustrated in Figure 3, and as such, would also understand how and what confidence factors are assigned. Accordingly, Applicants respectfully submit that Claims 3 and 13 overcome the Section 112 first paragraph rejections.

With respect to Claims 4 and 14, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand the freeze threshold value and the fault threshold value without illustrating their values within the Figures. Accordingly, Applicants respectfully submit that Claims 4 and 14 overcome the Section 112 first paragraph rejections.

With respect to Claim 5, Claim 5 depends from Claim 1 is submitted to overcome the Section 112 rejections. Accordingly, Applicants respectfully submit that Claim 5 overcomes the Section 112 first paragraph rejections.

With respect to Claim 6, as explained above, Applicants respectfully submit that illustrating a comparator is not necessary for an understanding of the invention. Rather, as recited in the specification at page 4, in one embodiment, a comparator may be coupled to the

logic circuit. Accordingly, Applicants respectfully submit that Claim 6 overcomes the Section 112 first paragraph rejections.

With respect to Claims 7-10, Claims 7-10 depend from Claim 6 which is submitted to overcome the Section 112 rejections. Accordingly, Applicants respectfully submit that Claims 7-10 overcome the Section 112 first paragraph rejections.

With respect to Claim 15, Applicants respectfully submit that one skilled in the art reading the disclosure, including the Figures, would understand what determines the difference of the first and second voltages exceeds a freeze or a fault threshold. Accordingly Applicants respectfully submit that Claim 15 overcomes the Section 112 first paragraph rejections.

With respect to Claims 16-18, Claims 16-18 depend from Claim 15 which is submitted to overcome the Section 112 rejections. Accordingly, Applicants respectfully submit that Claims 16-18 overcome the Section 112 first paragraph rejections.

With respect to Claims 3-4 and 11-14, Applicants respectfully submit that Claims 3, 4, and 14 have been amended to overcome the Section 112 second paragraph rejections. More specifically, Claim 3 has been amended to recite "a confidence factor that a fault", and Claims 4, and 14 have been amended to recite "approximately equal".

With respect to Claim 11, as explained above, Applicants respectfully submit that an artisian of ordinary skill in the art reading the disclosure, including the Figures, would understand the phrase "maintaining the reference value constant". Claims 12 and 13 depend from Claim 11, which is submitted to overcome the Section 112 second paragraph rejections.

For the reasons set forth above, Applicants respectfully request that the Section 112 rejection of Claims 1-18 be withdrawn.

The rejection of Claims 1-3, 5-7, 9, 11-13, 15, and 19under 35 U.S.C. § 102(b) as being anticipated by Maher is respectfully traversed

Maher describes a variable differential transformer system 10 that includes a linear and a rotary path (L/RVDT). System 10 includes two short term filter stages that include a resistor R_{fl1} and a capacitor C_{fl1}. System 10 also includes a long term filter stage that includes a comparator CM3, resistors R35, R36, and R37, and a Capacitor C_{fau}. A DC component is supplied to a negative input of comparator CM3 to determine primary coil faults and short circuit faults. The DC component reference signals supplied to comparator CM3 are compared to fault thresholds, and if the difference between the signal values exceeds or is below the threshold, CM3 transmits a signal indicative of a fault.

Claim 1 recites a method for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the method comprises the steps of "summing the voltage outputs to obtain a summed voltage value...if an absolute value of the difference between a current value of the summed voltage value and the reference value exceeds a freeze threshold, then maintaining the reference value constant."

Maher does not describe nor suggest a method for detecting faults in a transducer including a secondary winding having at least two voltage outputs, in combination with method steps including summing the voltage outputs to obtain a summed voltage value, and if an absolute value of the difference between a current value of the summed voltage value and the reference value exceeds a freeze threshold, then maintaining the reference value constant. Specifically, Maher does not describe nor suggest determining an absolute value of the difference between a current value of the summed voltage value and the reference value. Furthermore, Maher does not describe nor suggest maintaining the reference value constant. For the reasons set forth above, Claim 1 is submitted to be patentable over Maher.

Claims 2, 3, and 5 depend, directly or indirectly, from independent Claim 1. When the recitations of Claims 2, 3, and 5 are considered in combination with the recitations of Claim 1, Applicants submit that dependent Claims 2, 3, and 5 likewise are patentable over Maher.

Claim 6 recites an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, the apparatus comprising "a short term filter...a long term filter...at least one of said short term filter and said long term filter comprises a one pole lag filter...." Maher does not describe nor suggest an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus includes a short term filter and a long term filter, wherein at least one of said short term filter and said long term filter comprises a one pole lag filter. Specifically, Maher does not describe nor suggest an apparatus including a one pole lag filter. For the reasons set forth above, Claim 6 is submitted to be patentable over Maher.

Claims 7, 9, and 11-13 depend, directly or indirectly, from independent Claim 6. When the recitations of Claims 7, 9, and 11-13 are considered in combination with the recitations of Claim 6, Applicants submit that dependent Claims 7, 9, and 11-13 likewise are patentable over Maher.

Claim 15 recites an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus comprises "a short term filter...said short term filter comprising a one pole lag filter...a long term filter...said long term filter comprising a one pole lag filter...a comparator for generating a difference signal representative of a difference between the first voltage value and the second voltage value, if an absolute value of the difference between the first voltage value and the second voltage value exceeds a freeze threshold, then said long term filter maintains said second voltage value constant, and if the absolute value of the difference between the first voltage value and the second voltage value exceeds a fault threshold, then said apparatus generates a fault indicator signal.

Maher does not describe nor suggest an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus includes a short term filter that is one pole lag filter, a long term filter that is a one pole lag filter,

and a comparator that generates a difference signal representative of a difference between the first voltage value and the second voltage value, wherein if an absolute value of the difference between the first voltage value and the second voltage value exceeds a freeze threshold, then the long term filter maintains the second voltage value constant, and if the absolute value of the difference between the first voltage value and the second voltage value exceeds a fault threshold, then the apparatus generates a fault indicator signal. Specifically, Maher does not describe nor suggest an apparatus including a short and long term filter that are one pole lag filters, and a comparator that determines an absolute value of the difference between the first and second voltage values, wherein the long term filter may maintain the second voltage constant. For the reasons set forth above, Claim 15 is submitted to be patentable over Maher.

Claim 18 depends from independent Claim 15. When the recitations of Claim 18 are considered in combination with the recitations of Claim 15, Applicants submit that dependent Claim 18 likewise is patentable over Maher.

For the reasons set forth above, Applicants respectfully request that the Section 102 rejection of Claims 1-3, 5-7, 9, 11-13, 15, and 18 be withdrawn.

The rejection of Claims 4, 8, 10, 14, 16, and 17 under 35 U.S.C. § 103 as being unpatentable over Maher is respectfully traversed.

Maher is described above. Applicants respectfully submit that the Section 103 rejection of the presently pending claims is not a proper rejection. As is well established, the mere assertion that it would have been obvious to one of ordinary skill in the art to have modified Maher to obtain the claimed recitations of the present invention does not support a prima facia obvious rejection. Rather, each allegation of what would have been an obvious matter of design choice must always be supported by citation to some reference work recognized as standard in the pertinent art and the Applicants given the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference. Applicants have not been provided with the citation to any reference supporting the combination made in the rejection. The

design choice

rejection, therefore, fails to provide the Applicants with a fair opportunity to respond to the rejection, and fails to provide the Applicants with the opportunity to challenge the correctness of the rejection. Obviousness cannot be established by merely suggesting that it would have been obvious to modify

Further, and to the extent understood, Maher does not describe nor suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited combination. Specifically, Claim 4 depends from Claim 1 which recites a method for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the method comprises the steps of "summing the voltage outputs to obtain a summed voltage value...if an absolute value of the difference between a current value of the summed voltage value and the reference value exceeds a freeze threshold, then maintaining the reference value constant."

Maher does not describe nor suggest a method for detecting faults in a transducer including a secondary winding having at least two voltage outputs, in combination with method steps including summing the voltage outputs to obtain a summed voltage value, and if an absolute value of the difference between a current value of the summed voltage value and the reference value exceeds a freeze threshold, then maintaining the reference value constant. Specifically, Maher does not describe nor suggest determining an absolute value of the difference between a current value of the summed voltage value and the reference value. Furthermore, Maher does not describe nor suggest maintaining the reference value constant. For the reasons set forth above, Claim 1 is submitted to be patentable over Maher.

Claim 4 depends from independent Claim 1. When the recitations of Claim 4 are considered in combination with the recitations of Claim 1, Applicants submit that dependent Claim 4 likewise is patentable over Maher.

Claims 8, 10, and 14 depend from Claim 6 which recites an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, the apparatus

comprising "a short term filter...a long term filter...at least one of said short term filter and said long term filter comprises a one pole lag filter...." Maher does not describe nor suggest an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus includes a short term filter and a long term filter, wherein at least one of said short term filter and said long term filter comprises a one pole lag filter. Specifically, Maher does not describe nor suggest an apparatus including a one pole lag filter. For the reasons set forth above, Claim 6 is submitted to be patentable over Maher.

Claims 8, 10, and 14 depend, directly or indirectly, from independent Claim 6. When the recitations of Claims 8, 10, and 14 are considered in combination with the recitations of Claim 6, Applicants submit that dependent Claims 8, 10, and 14 likewise are patentable over Maher.

Claims 16 and 17 depend from Claim 15 which recites an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus comprises "a short term filter...said short term filter comprising a one pole lag filter...a long term filter...said long term filter comprising a one pole lag filter...a comparator for generating a difference signal representative of a difference between the first voltage value and the second voltage value, if an absolute value of the difference between the first voltage value and the second voltage value exceeds a freeze threshold, then said long term filter maintains said second voltage value constant, and if the absolute value of the difference between the first voltage value and the second voltage value exceeds a fault threshold, then said apparatus generates a fault indicator signal.

Maher does not describe nor suggest an apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, wherein the apparatus includes a short term filter that is one pole lag filter, a long term filter that is a one pole lag filter, and a comparator that generates a difference signal representative of a difference between the first voltage value and the second voltage value, wherein if an absolute value of the difference between the first voltage value and the second voltage value exceeds a freeze threshold, then the

long term filter maintains the second voltage value constant, and if the absolute value of the difference between the first voltage value and the second voltage value exceeds a fault threshold, then the apparatus generates a fault indicator signal. Specifically, Maher does not describe nor suggest an apparatus including a short and long term filter that are one pole lag filters, and a comparator that determines an absolute value of the difference between the first and second voltage values, wherein the long term filter may maintain the second voltage constant. For the reasons set forth above, Claim 15 is submitted to be patentable over Maher.

Claims 16 and 17 depend from independent Claim 15. When the recitations of Claims 16 and 17 are considered in combination with the recitations of Claim 15, Applicants submit that dependent Claims 16 and 17 likewise are patentable over Maher.

For the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 4, 8, 10, 14, 16, and 17 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

This paper is filed by the undersigned, who is not presently an attorney of record, pursuant to 37 C.F.R. 1.34(a), MPEP 405, at the instruction of the attorney of record.

Respectfully Submitted,

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cook et al.

Serial No.: ~~09/552,563~~ 09/522,563

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Art Unit: 2858

Examiner: Patel, P.

CERTIFICATE OF MAILING

I certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on July 25, 2001.

Robert B. Reeser III
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SUBMISSION OF MARKED UP PARAGRAPHS AND CLAIMS

Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Submitted herewith are marked up paragraphs and Claims in accordance with 37 C.F.R. 1.121(b)(1)(ii) and 37 C.F.R. 1.121(c)(1)(ii)

IN THE TITLE

Please delete the title and replace it with the following replacement title:

DETECTION OF FAULTS IN LINEAR AND ROTARY VOLTAGE TRANSDUCERS

IN THE SPECIFICATION

Please delete the paragraph beginning on page 3 at line 17 and ending on page 3 at line 26, and replace with the following replacement paragraph:

Short term filter 52 includes a multiplier 56 which multiplies the summed value by a short term weight factor 58. In an exemplary embodiment, the short term weight factor KST is 0.1. The weighted sum is then added at a summer 60 with a weighted value from a most previous sum. Specifically, the [most] previous short term sum value 62 is multiplied at a multiplier 64 by a weighting factor 66. In the exemplary embodiment, this weighting factor is 0.9. This weighted value is added at summer 60 with the current weighted value to provide a short term sum value. This current short term sum value is supplied to a summer 68. The current short term sum value also is stored in memory (not shown) so that it can be used in determining the next current short term sum value.

Please delete the paragraphs beginning on page 4 at line 3 and ending on page 5 at line 21, and replace with the following replacement paragraphs:

More specifically, long term filter 54 includes a multiplier 70 which multiplies the summed value by a long term weight factor 72. In an exemplary embodiment, the long term weight factor KLT is 0.0005. The weighted sum is then added at a summer 74 with a weighted value from a most previous sum. Specifically, the [most] previous long term sum value 76 is multiplied at a multiplier 78 by a weighting factor 80. In the exemplary embodiment, this weighting factor is 0.9995. This weighted value is added at summer 74 with the current weighted value to provide a long term sum value. This long term sum value is supplied to summer 68. The current long term sum value also is stored in memory (not shown) so that it can be used in determining the next current [short] long term sum value. In one embodiment, a comparator (not shown) is coupled to summer 68.

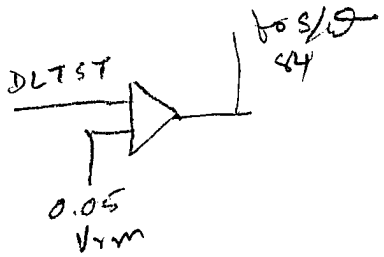
Again, the output of short term filter 52 is continuously summed at summer 68 with the output of long term filter 54. An absolute value 82 of this sum is obtained and is designated as DLTST (i.e., difference between long term and short term filters 52 and 54. Depending upon the value of DLTST, certain actions may be taken as described below.

Specifically, in an exemplary embodiment, if the absolute value of DLTST exceeds 0.05 Vrms, then the output of long term filter 54 should be frozen, i.e., a control signal 84 should transition switch S from position 0 to position 1. This results in freezing the value of long term filter and the reference value from long term filter 54 remains constant, i.e., value 76. This relationship is represented below.

If DLTST > LTfreezeThresh

Then LTfreeze = 1

Else LTfreeze = 0,



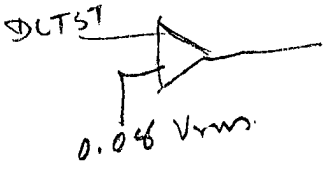
where, LTfreezeThresh = 0.05, and where LtfreezeThresh represents a long term filter freeze threshold.

If the absolute value of [DLST] DLTST exceeds 0.08 Vrms, then a fault indication VDTFLT should be set. This relationship is represented below.

If DLTST > V1 + V2FLTThresh,

Then VDTFLT = 1,

Else VDTFLT = 0,



where, V1 + V2FLTThresh = 0.08, and where V2FLTThresh represents a fault threshold value.

If the absolute value of [DLST] DLTST is less than 0.08 Vrms, the fault indication should not be set. As the absolute value of DLTST changes between 0.04 Vrms and 0.08 Vrms, a confidence factor is generated which varies between 1.0 and 0.0, respectively. For absolute values of [DLST] DLTST less than 0.04 Vrms, the confidence factor should be 1.0, e.g., confident that no fault has occurred. For absolute values of DLTST values greater than 0.08

Vrms, the confidence factor should be 0.0, e.g., not confident that no fault has occurred. The confidence factor can be utilized in a control system to minimize the effect of an LVDT / RVDT failure.

An exemplary confidence factor is illustrated in a graph shown in Figure 3. As shown in Figure 3, when the Vrms value of the absolute value of DLTST is less than CFHiThresh, then a confidence [value] factor of 1 is assigned. When the Vrms value of the absolute value of DLTST is greater than CFLoThresh, then a confidence factor of 0 is assigned. For Vrms values of the absolute value of DLTST between CFHiThresh and CFLoThresh, a linear relationship between the Vrms value and the confidence factor is provided. Exemplary values of CFHiThresh and CFLoThresh are set forth below.

IN THE CLAIMS

3. (once amended) A method in accordance with Claim 2 wherein if the absolute value of the difference between a current value of the summed voltage value and the reference value is less than the fault threshold, then generating a confidence factor [indicative of a likelihood that] representing that a fault has occurred.

4. (once amended) A method in accordance with Claim 3 wherein the freeze threshold value is [about] approximately equal 0.05 Vrms, and wherein the fault threshold value is [about] approximately equal 0.08 Vrms.

6. (once amended) Apparatus for detecting faults in a transducer including a secondary winding having at least two voltage outputs, said apparatus comprising:

a short term filter for generating a first voltage value representative of a current value of a sum of the secondary winding output voltages; and

a long term filter for generating a second voltage value representative of a non-faulted value of a sum of the secondary winding output voltages, at least one of said long term filter and said short term filter comprising a one pole lag filter; and

a comparator for generating a difference signal representative of a difference between the first voltage value and the second voltage value.

14. (once amended) Apparatus in accordance with Claim 12 wherein the freeze threshold value is [about] approximately equal 0.05 Vrms, and wherein the fault threshold value is [about] approximately equal 0.08 Vrms.

This paper is filed by the undersigned, who is not presently an attorney of record, pursuant to 37 C.F.R. 1.34(a), MPEP 405, at the instruction of the attorney of record.

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